Introduction to Digital Systems

Course Code:

CSE 224

Course Period:

Spring

Course Type:

Core

Credits:

4

Theoric:

3

Practice:

0

Laboratory Hour:

2

ECTS:

6

Prerequisite Courses:

Principles of Logic Design [1]
Course Language:

English

Course Objectives:

This practical, hands-on course introduces digital logic design, digital system design principles. Students first learn to design large-scale logic circuits from fundamental building blocks (data paths, adders, multipliers, memory) and methods based on FPGA design flow (register-transfer design, hardware description languages, design verification and simulation). Students also learn how to interface digital circuitry to analog hardware

domain. Finally, system on chip concepts are covered. Through a series of laboratory exercises using FPGA boards and microcontrollers, students acquire skills in the design/verification/implementation of digital systems.

Course Content:

The what/why/how of ICs, FPGAs, and ASIC Flow, MOS Transistors, CMOS Logic, CMOS Process. Verilog and basic digital design principles. Combinational logic, data path, adders, carry save trees, multipliers, priority encoders. Verilog and basic digital design principles, sequential logic, barrel shifter, counters. Design verification concepts, simulation. coverage. Scheduling. Pipelining. Resource sharing. Handshaking. UART, RS232, PS/2, I2C, SPI, VGA interfaces. Memory inference, FIFO, Block RAMs, external RAMs. CPU design, system-on-chip design. Analog-to-Digital Converters. Sensors, motor control, filters, Pulse Width Modulator, Digital-to-Analog Converters. Microcontrollers. 10 Laboratory exercises, one Term Project.

Course Methodology:

1: Lecture, 2: Question-Answer, 3: Lab, 4: Case-study

Course Evaluation Methods:

A: Testing, B: Experiment, C: Homework, D: Project

Course Learning Outcomes	**Program Learning Outcomes**	**Teaching Methods**	**Assessment Methods**
1) Adequate knowledge in digital electronics and digital design concepts.	1,2,3,4,5	1,2	A, B, C, D
2) Ability to design and implement digital circuits under realistic constraints and conditions.	1,2,3,4,5	1,2,3	B, D
3) Ability to debug, verify, simulate digital circuits.	4,5	1,2,3	B, D
4) Ability to devise, select, and use modern techniques and tools needed for digital design.	4,5	1,2,3	B, D
5) Ability to work in a team.	6	3	B, D

COURSE CONTENT

Week	Topics	Study Materials
1	THE WHAT/WHY/HOW OF ICS, FPGAS, AND ASIC FLOW. MOS TRANSISTORS. CMOS LOGIC. CMOS PROCESS.	Textbook
2	VERILOG AND BASIC DIGITAL DESIGN PRINCIPLES. COMBINATIONAL LOGIC. DATA PATH. ADDERS, CARRY SAVE TREES, MULTIPLIERS, PRIORITY ENCODERS. XILINX ISE.	Textbook
3	VERILOG AND BASIC DIGITAL DESIGN PRINCIPLES. SEQUENTIAL LOGIC. COUNTERS. FINITE STATE MACHINES. SIMPLE CPU DESIGN.	Textbook
4	DESIGN VERIFICATION CONCEPTS. SIMULATION. COVERAGE.	Textbook
5	MIDTERM I	Textbook
6	DIGITAL DESIGN PRINCIPLES. SCHEDULING. PIPELINING. RESOURCE SHARING. HAND SHAKING	Textbook
7	UART, RS232, I2C, SPI PROTOCOLS.	Textbook
8	PS/2 MOUSE/KEYBOARD INTERFACE.	Textbook
9	MEMORY INFERENCE, FIFO, BLOCK RAMS, EXTERNAL RAMS. IP CORE GENERATOR. VGA.	Textbook
10	VGA	Textbook
11	SENSORS, ADC, DAC PWM, MOTOR CONTROL	Textbook
12	SYSTEM ON CHIP CONCEPTS. MICROCONTROLLERS	Textbook
13	MIDTERM EXAM II	Textbook
14	PROJECT DEMOS	–

RECOMMENDED SOURCES

Textbook

FPGA PROTOTYPİNG BY VERILOG EXAMPLES BY PONG P. CHU, WILEY

Additional Resources	THE ART OF HARDWARE ARCHITECTURE, MOHIT ARORA, SPRINGER A BAKER'S DOZEN REAL ANALOG SOLUTIONS FOR DIGİTAL DESIGNERS BY BONNIE BAKER, ELSEVIER THE VERILOG HARDWARE DESCRIPTION LANGUAGE, FIFTH EDITION BY D. E. THOMAS

MATERIAL SHARING

Documents	http://coadsys.yeditepe.edu.tr/ [2]
Assignments	http://coadsys.yeditepe.edu.tr/ [2]
Exams	http://coadsys.yeditepe.edu.tr/ [2]

ASSESSMENT

IN-TERM STUDIES	**NUMBER**	**PERCENTAGE**
Mid-terms	2	50
Assignment	2	10
Lab Work	10	10
Term Project	1	30
Total		**100**
CONTRIBUTION OF FINAL EXAMINATION TO OVERALL GRADE		30
CONTRIBUTION OF IN-TERM STUDIES TO OVERALL GRADE		70
Total		**100**

COURSE'S CONTRIBUTION TO PROGRAM

No	Program Learning Outcomes	1	2	3	**4**	5
1	Adequate knowledge in mathematics, science and engineering subjects pertaining to the relevant discipline; ability to use theoretical and applied information in these areas to model and solve engineering problems.				**X**	
2	Ability to identify, formulate, and solve complex engineering problems; ability to select and apply proper analysis and modeling methods for this purpose.					**X**

3	Ability to design a complex system, process, device or product under realistic constraints and conditions, in such a way as to meet the desired result; ability to apply modern design methods for this purpose.	**X**
4	Ability to devise, select, and use modern techniques and tools needed for engineering practice; ability to employ information technologies effectively.	**X**
5	Ability to design and conduct experiments, gather data, analyze and interpret results for investigating engineering problems.	**X**
6	Ability to work efficiently in intra-disciplinary and multi-disciplinary teams; ability to work individually.	**X**
7	Ability to communicate effectively both orally and in writing; knowledge of a minimum of one foreign language.	
8	Recognition of the need for lifelong learning; ability to access information, to follow developments in science and technology, and to continue to educate him/herself.	
9	Awareness of professional and ethical responsibility.	
10	Information about business life practices such as project management, risk management, and change management; awareness of entrepreneurship, innovation, and sustainable development.	
11	Knowledge about contemporary issues and the global and societal effects of engineering practices on health, environment, and safety; awareness of the legal consequences of engineering solutions.	

ECTS ALLOCATED BASED ON STUDENT WORKLOAD BY THE COURSE DESCRIPTION

Activities	Quantity	Duration (Hour)	Total Workload (Hour)
Course Duration	14	5	70
Hours for off-the-classroom study (Pre-study, practice)	14	2	28
Midterm examination	2	2	4
Homework	2	2	4
Project	1	30	30
Final examination	1	3	3

Total Work Load	139
Total Work Load / 25 (h)	5.56
ECTS Credit of the Course	6