# Digital System Design

Course Code:

CSE 425

Course Period:

Autumn

Course Type:

Area Elective

Credits:

3

Theoric:

3

Practice:

0

Laboratory Hour:

0

ECTS:

5

Prerequisite Courses:

Principles of Logic Design [1]
Course Language:

English

Course Objectives:

This practical, hands-on course introduces digital logic design, system-level design using current state of the art in EDA tools used by professionals in VLSI field today. Students learn to design large-scale logic circuits from fundamental building blocks and methods. This course focuses mostly on the front-end techniques involved in ASIC/FPGA design flow, but also gives a brief introduction of CMOS process and CMOS logic. Through a series of laboratory exercises using FPGA boards, students will acquire skills in the design/verification/implementation of digital systems.

Course Content:

The what/why/how of ICs, FPGAs, and ASIC Flow, MOS Transistors, CMOS Logic, CMOS Process. Verilog and basic digital design principles. Data paths, adders, multipliers, memory, embedded-processors, IPs. Behavioral design specification, system partitioning, register-transfer design, hardware description languages (Verilog, VHDL), pipelining, parallelism, resource sharing, hand shaking, design verification, and simulation, high level verification languages, code coverage, high-level synthesis, FPGA prototyping, gate-level timing, test generation, design for testability. Laboratory exercises, one Term Project.

Course Methodology:

1: Lecture, 2: Question-Answer, 3: Lab, 4: Case-study

Course Evaluation Methods:

A: Testing, B: Experiment, C: Homework, D: Project

| Course Learning Outcomes | Program Learning Outcomes | Teaching Methods | Assessment Methods |
|---|---|---|---|
| 1) Adequate knowledge in digital system design concepts. | 1,2,3,4,5 | 1,2 | A,B,C,D |
| 2) Ability to design and implement digital circuits under realistic constraints and conditions. | 1,2,3,4,5 | 1,2,3 | B,D |
| 3) Ability to debug, verify, simulate, synthesize digital circuits. | 4,5 | 1,2,3 | B,D |
| 4) Ability to devise, select, and use modern techniques and tools needed for digital system design. | 4,5 | 1,2,3 | B,D |
| 5) Ability to work in a team. | 6 | 3 | B,D |

**COURSE CONTENT**

| Week | Topics | Study Materials |
|---|---|---|
| 1 | THE WHAT/WHY/HOW OF ICS, FPGAS, AND ASIC FLOW. FULL-CUSTOM, SEMI-CUSTOM, STANDARD CELL VLSI DESIGN. | Textbook |
| 2 | MOS TRANSISTORS. CMOS LOGIC. CMOS PROCESS. INTRO. VLSI LAYOUT SYNTHESIS. DRC. LVS. | |

| | | |
|---|---|---|
| 3 | VERILOG AND BASIC DIGITAL DESIGN PRINCIPLES. BEHAVIORAL AND RTL DESIGN ENTRY | Textbook |
| 4 | COMBINATIONAL & SEQUENTIAL DIGITAL DESIGN. FSM. INTRO. COMP. ARITHMETIC. DATA PATH. ADDERS. MULTIPLIERS. IPs. | Textbook |
| 5 | DESIGN VERIFICATION CONCEPTS. SIMULATION. COVERAGE. | Textbook |
| 6 | MIDTERM I | Textbook |
| 7 | SCHEDULING. PIPELINING. RESOURCE SHARING. HAND SHAKING | Textbook |
| 8 | MULTIPLE CLOCK DOMAINS. ASYNC/SYNCH FIFO. METASTABILITY ISSUES. | Textbook |
| 9 | HIGH LEVEL SYNTHESIS.  GATE LEVEL TIMING. | Textbook |
| 10 | MEMORY INFERENCE, FIFO, BLOCK RAMS, EXTERNAL RAMS. IP CORE GENERATOR. | Textbook |
| 11 | RS232, VGA, HDMI, LCD, SPI, PCI, I2C | Textbook |
| 12 | TEST AUTOMATION. INTRO. VLSI TEST (MANUFACTURING TEST), DESIGN FOR TESTABILITY, ATPG. | Textbook |
| 13 | MIDTERM EXAM II | Textbook |
| 14 | PROJECT DEMOS | – |

## RECOMMENDED SOURCES

| | |
|---|---|
| **Textbook** | MODERN VLSI DESIGN BY WAYNE WOLF, PRENTICE-HALL |
| **Additional Resources** | ART OF HARDWARE ARCHITECTURE BY MOHIT ARORA, SPRINGER<br><br>FPGA PROTOTYPING BY VERILOG EXAMPLES BY PONG P. CHU, WILEY. |

## MATERIAL SHARING

| | |
|---|---|
| **Documents** | coadsys.yeditepe.edu.tr/ |
| **Assignments** | coadsys.yeditepe.edu.tr/ |
| **Exams** | coadsys.yeditepe.edu.tr/ |

## ASSESSMENT

| IN-TERM STUDIES | NUMBER | PERCENTAGE |
|---|---|---|
| Mid-terms | 2 | 50 |
| Assignment | 2 | 5 |
| Lab Work | 10 | 15 |
| Term Project | 1 | 30 |
| **Total** | | **100** |
| **CONTRIBUTION OF FINAL EXAMINATION TO OVERALL GRADE** | | 30 |
| **CONTRIBUTION OF IN-TERM STUDIES TO OVERALL GRADE** | | 70 |
| **Total** | | **100** |

## COURSE'S CONTRIBUTION TO PROGRAM

| No | Program Learning Outcomes | Contribution | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| 1 | Adequate knowledge in mathematics, science and engineering subjects pertaining to the relevant discipline; ability to use theoretical and applied information in these areas to model and solve engineering problems. | | | | | | **X** |
| 2 | Ability to identify, formulate, and solve complex engineering problems; ability to select and apply proper analysis and modeling methods for this purpose. | | | | | | **X** |
| 3 | Ability to design a complex system, process, device or product under realistic constraints and conditions, in such a way as to meet the desired result; ability to apply modern design methods for this purpose. | | | | | | **X** |
| 4 | Ability to devise, select, and use modern techniques and tools needed for engineering practice; ability to employ information technologies effectively. | | | | | | **X** |
| 5 | Ability to design and conduct experiments, gather data, analyze and interpret results for investigating engineering problems. | | | | | | **X** |
| 6 | Ability to work efficiently in intra-disciplinary and multi-disciplinary teams; ability to work individually. | | | | | | **X** |

| | | |
|---|---|---|
| 7 | Ability to communicate effectively both orally and in writing; knowledge of a minimum of one foreign language. | **X** |
| 8 | Recognition of the need for lifelong learning; ability to access information, to follow developments in science and technology, and to continue to educate him/herself. | **X** |
| 9 | Awareness of professional and ethical responsibility. | **X** |
| 10 | Information about business life practices such as project management, risk management, and change management; awareness of entrepreneurship, innovation, and sustainable development. | **X** |
| 11 | Knowledge about contemporary issues and the global and societal effects of engineering practices on health, environment, and safety; awareness of the legal consequences of engineering solutions. | **X** |

**ECTS ALLOCATED BASED ON STUDENT WORKLOAD BY THE COURSE DESCRIPTION**

| Activities | Quantity | Duration (Hour) | Total Workload (Hour) |
|---|---|---|---|
| Course Duration (Excluding the exam weeks: 12x Total course hours) | 12 | 3 | 36 |
| Hours for off-the-classroom study (Pre-study, practice) | 14 | 2 | 28 |
| Midterm examination | 2 | 4 | 8 |
| Homework | 2 | 4 | 8 |
| Project | 1 | 40 | 40 |
| Final examination | 1 | 6 | 6 |
| **Total Work Load** | | | 126 |
| **Total Work Load / 25 (h)** | | | 4.85 |
| **ECTS Credit of the Course** | | | 5 |