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CDTA-Based Capacitance Multipliers

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Abstract

Two grounded capacitance multipliers employing the current differencing transconductance amplifier (CDTA) are proposed. They can be easily modified to the floating versions by using an additional difference voltage amplifier. Each multiplier contains one CDTA, one capacitor, pseudo-grounded via a low-impedance CDTA input terminal, and one or two resistors. A careful error analysis is made and both circuits are compared in terms of their benefits and drawbacks. The results of the measurements on the specimens exploiting on-chip CDTAs correspond to the design objectives.

Keywords CDTA · Capacitance multiplier · Current amplifier · Symbolic analysis · Error analysis · Simulation · Measurement

1 Introduction

A capacitance multiplier (CM) is a circuit that is used to realize a much larger capacitance value by using a small physical capacitance. These circuits are important parts of integrated circuit (IC) design and fabrication technologies where it is possible to emulate relatively large capacitance values although physically realizable capacitances are limited to a few picofarads. For example, in a typical digital CMOS fabrication process, realizing a physically large capacitor on the IC is very costly in any IC process unless special fabrication process steps have been added to implement it [39]. In the specific case of CMOS image sensor, the capacitor should be in the range of several

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hundreds of picofarads up to a few nanofarads, which presents a major fabrication obstacle when creating a large noise attenuating capacitor. Due to limited space on the IC die, the physical size of the capacitor needed becomes prohibitive.

In another case of the integration of a PLL loop filter, especially a zero-making capacitor requiring the largest capacitance value is a challenging task when implementing a monolithic PLL frequency synthesizer [8]. Using the Miller effect, while the capacitance multiplication factor is practically limited in the voltage mode, the current-mode topology offers the possibility of achieving higher multiplication factors [14, 32].

Various CM designs have been presented in the literature. For example, a simple CM comprises a Miller capacitor structure C_{MS} coupled between the collector and base electrodes of an integrated NPN transistor with an effective capacitance between the base and ground having an original C_{MS} value multiplied by a factor which depends on the transistor's gain [10]. Since the resultant capacitance is a function of the beta of the transistor, it becomes strongly temperature dependent. Enhanced current-mode Miller compensation techniques and resulting CM structures were reported in [8, 14, 22, 27, 32].

Other CM designs implement operational amplifiers [2], operational transconductance amplifiers (OTAs) [15, 20], current conveyors (CCs) [1, 18, 21, 37], modified current feedback operational amplifiers (CFOAs) [38], differential input buffered and transconductance amplifiers (DBTAs) [36], differential difference current conveyors (DDCCs) [26], fully differential current conveyors (FDCCs) [12], current conveyor transconductance amplifiers (CCTAs) [16, 30], current mirrors and current amplifiers (CMs and CAs) [7, 24, 25, 29], dual-X current conveyor (DXCCII) [23], and other active building blocks and their combinations [3, 9, 11, 13, 31]. Each of these designs has advantages, as well as disadvantages.

The following points need to be considered for a good CM design:

(1) Employment of the minimum number of active elements. (2) Avoiding excessive use of passive components. (3) Possibility of electronic tuning. (4) The minimum amount of low-frequency restrictions.

The principle of the majority of hitherto published CMs can be described by the diagrams in Fig. 1.

For the grounded version, the terminal voltage of the emulated capacitor is processed by the derivative voltage-to-current converter, frequently implemented as a grounded capacitor with the capacitance C. Its current is subsequently amplified B times via a current amplifier. The amplified current is directed such that it is in phase with the current flowing through the passive capacitor. The resulting circuit in Fig. 1a emulates a capacitor with the capacitance $C_{\text{mul}} = (B+1)C$; thus, the multiplication factor is $B+1$.

The emulator of the floating capacitor in Fig. 1b is completed with a high-input impedance difference voltage amplifier with the gain A. The current amplifier has bipolar outputs. The capacitance of the emulated capacitor is then $C_{\text{mul}} = ABC$; thus, the multiplication factor is AB.

For the common case of $A = 1$, which provides the maximum possible dynamic range of the voltage, the multiplying effect is accomplished only via a current gain of the block B. The block A is frequently implemented by the voltage stage of the DVCC

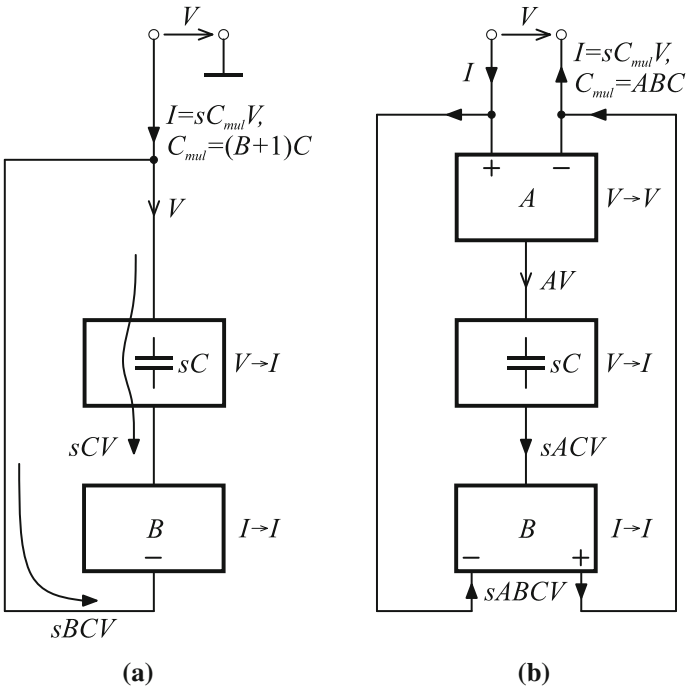

Fig. 1 A diagram of the **a** grounded, **b** floating capacitance multiplier

[3, 31], DDCC [26], or OTA [15]. The differentiating voltage–current converter and the current sensor are frequently solved using the current conveyors, when the current of the x terminal, the grounded capacitor being connected to it, is conveyed into the z terminal [31]. The gain AB can be governed either by the gain A [22] or by the gain of the current–current amplifier, for example, by two CCCIIs in cascade connection [31], by the COA [13], or via two OTAs [15]. The circuitry from [15] is temperature independent.

An interesting modification of the principle from Fig. 1b is described in [15]. The input part is formed via the OTA (voltage-to-current converter), which is loaded by the synthetic inductor (two OTAs and one capacitor). The inductor implements the differentiating current-to-voltage converter. The voltage then drives the bipolar-output OTA, which supplies the input terminals.

The current differencing transconductance amplifier (CDTA) has been one of the most frequently studied active building blocks in the last decade [4, 5, 17, 28, 33–35]. However, we have noted that no CDTA-based CM circuits have been reported in the literature. Therefore, the main objective of this paper is to present CDTA-based CMs using different circuits based on the concept in Fig. 1 as a further verification of the fact that CDTA is a universal and versatile active element. It turns out that the CDTA provides the effective design of grounded CMs. On the other hand, as Fig. 1b indicates, the floating multiplier requires an auxiliary circuit with difference voltage

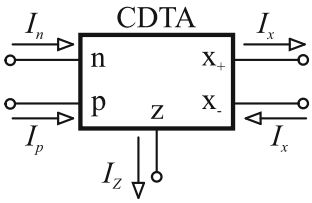

Fig. 2 Schematic symbol of the CDTA

input because the CDTA does not provide high-impedance sensing of the terminal voltage.

2 CDTA

The CDTA, whose schematic symbol is shown in Fig. 2, is an active circuit element introduced in [4]. Its parasitic input capacitances produce negligible effect due to low impedance levels. The CDTA can operate in a wide frequency range due to its current-input current-output mode of operation.

The low-impedance input stage is driven by two currents, I_p and I_n, and their difference is transferred as the current I_z to the high-impedance z terminal. The correspondent voltage drop at the external impedance connected to the z terminal is then converted into the output currents I_x via multiple-output transconductance stages. Figure 2 shows a simple case of two bidirectional equal currents, which correspond to equal transconductances g_m of both stages.

3 CDTA-Based Capacitance Multipliers

Figure 3a shows the basic version of the grounded CM resulting from the conception in Fig. 1a. The capacitor C is pseudo-grounded via the low-impedance input terminal p of the CDTA, and in the ideal case, its current is proportional to the derivative of the terminal voltage V. This current is copied into the z terminal, causing a voltage drop on the resistor R. This voltage is transformed into the current I_x via the internal OTA. The CM works on the classical principle of the current bootstrap [20]: In addition to the capacitor current, also its copy multiplied by the corresponding factor flows from the source V. The emulated capacitance is therefore

$$C_{\text{mul}} = (1 + g_m R)C. \tag{1}$$

The multiplication factor is determined by the $g_m R$ product. It can be problematic from the point of view of the temperature behavior. In addition, the input impedance of the p terminal of the CDTA in series with a capacitor may affect the high-frequency behavior of the multiplier. The circuit (a) therefore does not bring much added value to the hitherto published circuit ideas which also start from the principle in Fig. 1a and use different active elements.

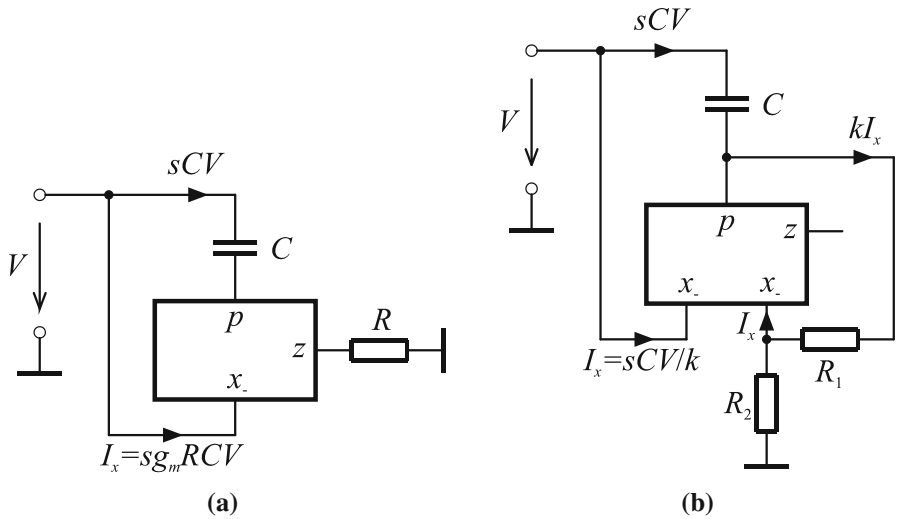

Fig. 3 Grounded CM employing the CDTA, **a** basic, **b** modified circuit

The circuit in Fig. 3b brings two improvements: The input impedance of p terminal is eliminated, and the CM operation is not sensitive to g_m and thus to temperature variations either. The z terminal is now disconnected and the current into the p terminal is therefore zero, which implies a zero voltage drop on its parasitic impedance. Such a regime is accomplished via negative feedback from the x output to the p input by means of the current divider R_1–R_2 which provides the transfer $k = R_1/(R_1 + R_2) < 1$. Since the capacitor current must be equal to the current through R_1, the emulated capacitance must be

$$C_{\text{mul}} = \left(1 + \frac{1}{k}\right)C = \left(2 + \frac{R_2}{R_1}\right)C. \tag{2}$$

The multiplication factor is therefore proportional to the attenuation of the current divider. A similar effect can be obtained without this divider via the CDTA, whose internal OTAs will have different transconductances. Then, the multiplication factor will depend on the g_m ratio.

According to Fig. 1b, the grounded CMs are extended to their floating versions in Fig. 4. The gain of the difference voltage amplifier should be preferably $A = 1$ in order to maximize the voltage swing and also the bandwidth.

The emulated capacitances for the versions **a** and **b** are given by Eqs. (3) and (4):

$$C_{\text{mul}} = g_m RCA, \tag{3}$$

$$C_{\text{mul}} = A\frac{C}{k} = AC\left(1 + \frac{R_2}{R_1}\right). \tag{4}$$

In comparison with version **a**, the version **b** provides the advantages discussed above.

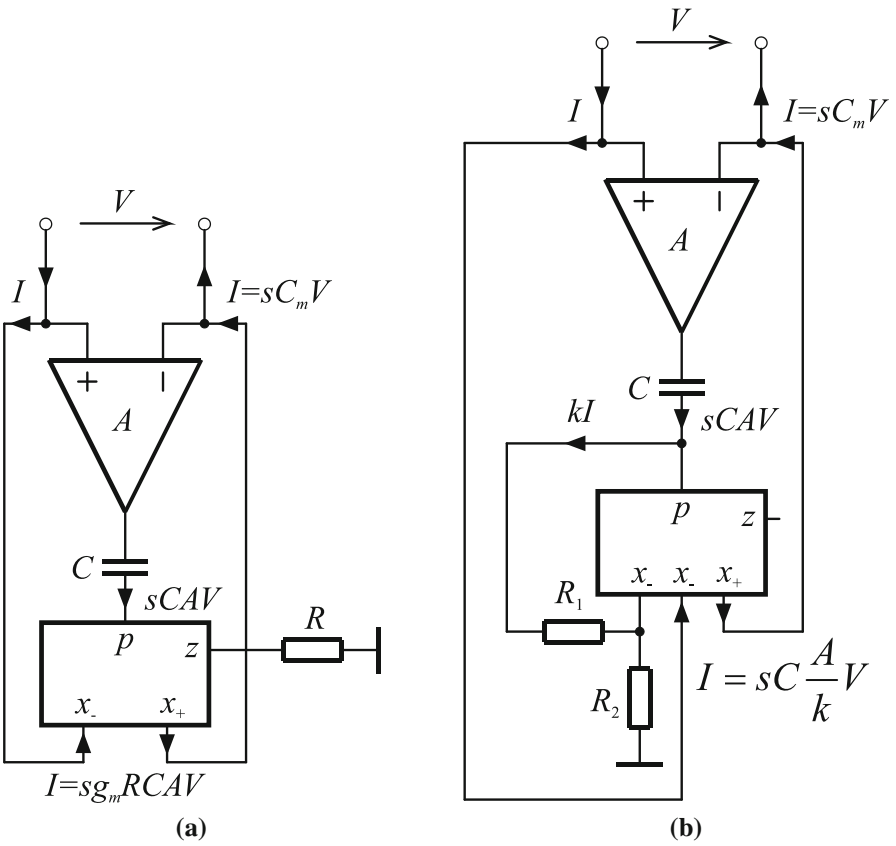

Fig. 4 Floating CM with difference voltage amplifier and CDTA, **a** basic, **b** modified circuit

Seeing that the floating versions in Fig. 4 start from the grounded CMs and extend them by the difference amplifier, we focus hereinafter on the error analysis and experiments with the CMs in Fig. 3, which are, in the context of hitherto published CMs, more interesting with regard to their simple circuit implementation.

4 Analysis of Non-ideal Case

4.1 Prerequisites for the Analysis

The linearized analysis of the impact of the CDTA parameters on the impedance emulated by the circuits from Fig. 3 is given below. The following CDTA parameters are considered:

Resistances R_p, R_z, R_x of terminals p (or n), z, and x, capacitances C_z and C_x of terminals z and x, DC transconductance g_{m0} and its 3-dB cutoff frequency $\omega_g = 2\pi f_g$ (single-pole model), current gain from p (or n) to z terminal (single-pole model, DC gain α_0, 3-dB cutoff frequency $\omega_\alpha = 2\pi f_\alpha$).

With respect to the subsequent experimental verification of the proposed circuits via an on-chip CDTA [6], the CDTA parameters extracted from the measurements were used for the error analysis:

$$R_p \approx 2.6\,\Omega,\ R_z \approx 2.1\,\mathrm{M}\Omega,\ R_x \approx 2.2\,\mathrm{M}\Omega,\ C_x \approx 10\,\mathrm{pF},\ C_z \approx 12\,\mathrm{pF},$$
$$g_{m0} = 1.22\,\mathrm{mS},\ \alpha_0 \approx 0.98,\ f_g \approx 10\,\mathrm{MHz},\ f_\alpha \approx 6\,\mathrm{MHz}.$$

The capacitor $C \approx 100$ pF was used for both CMs, and their operation was tested for various multiplication factors.

The linearized analysis was performed symbolically via the SNAP program, which also enables an SBG/SAG simplification of the generated symbolic formulae [19]. This way allows identifying key real influences and integrating them into compact models of the emulated impedances.

4.2 CM from Fig. 3a

The circuit from Fig. 3a was analyzed using the model from Sect. 4.1 for $R \approx 10$ kΩ. Then, according to Eq. (3), $C_{\mathrm{mul}} \approx 13C \approx 1.3$ nF. The symbolic formula for the impedance is the ratio of two s-domain polynomials of fourth order (the numerator) and fifth order (the denominator), whose coefficients are complicated functions of the CDTA parameters. The corresponding frequency dependences of the modulus and phases of the impedance are shown in Fig. 5a (red curves).

The low-frequency limitation (below ca 100 Hz) is caused by the parasitic resistance R_x of the x terminal of the CDTA, which works in parallel to the emulating gate. In the frequency range above ca 1 MHz, two factors take effect. The peak in the modulus of the impedance, accompanied by significant deformation of the phase response, is caused by finite bandwidths of the CDTA, namely by the cutoff frequencies of the current differencing unit ($f_\alpha \approx 6$ MHz) and OTA ($f_g \approx 10$ MHz). For the zero input resistance R_p, the impedance exhibits the $1/f$ drop (blue curve). The small resistance $R_p \approx 2.6\ \Omega$ causes the characteristic to shift toward the higher frequencies (green curve).

The symbolic formula for the admittance $Y = 1/Z$, which corresponds to the frequency characteristic for $R_p \approx 0$ (blue curve), models the CM behavior with a satisfactory precision up to ca 1 MHz:

$$Y = \frac{1}{R_x} + sC_x + sC\frac{1 + \alpha_0 g_{m0} R + sRC_z}{1 + sRC_z}. \tag{5}$$

Equation (5) can be arranged to the following form, which results in the model of the emulated impedance in Fig. 6:

$$Y = \frac{1}{R_x} + sC_x + sC + \frac{1}{\frac{1}{sC'} + R_\mathrm{s}}, \tag{6}$$

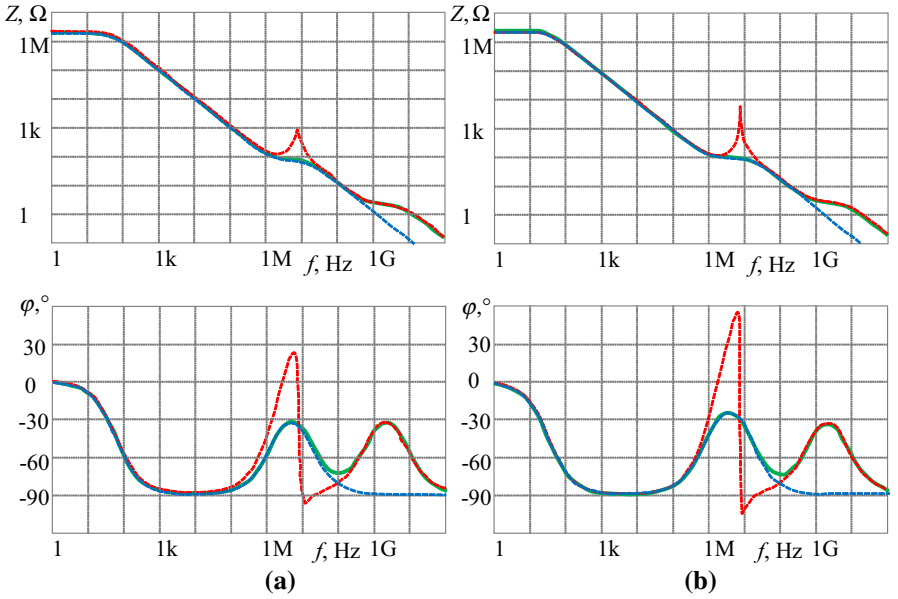

Fig. 5 Modulus and phase of the impedance emulated by the CM from **a** Fig. 3a, **b** Fig. 3b: red dashed line—complete model, green solid line—model with wideband CDTA ($\omega_\alpha \to \infty$, $\omega_g \to \infty$), blue dashed line—model with wideband CDTA and $R_p \to 0$ (Color figure online)

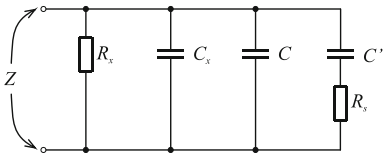

Fig. 6 Low-frequency model of the impedance emulated by CMs from Fig. 3

where

$$C' = \alpha_0 g_{m0} RC, \quad R_\mathrm{s} = \frac{C_z}{C\alpha_0 g_{m0}}. \tag{7}$$

The model in Fig. 6 confirms the influence of R_x and C_x on the low-frequency behavior of the impedance, which approaches the resistance R_x for $f \to 0$. Both the capacitance C_x and the additional capacitance $C' = C\alpha_0 g_{m0} R$ are added to the working capacitance C. It is in agreement with Eq. (3). The serial resistance R_s, which depends on the transconductance and the ratio of capacitances C_z and C according to Eq. (7), takes effect near the upper bound of the frequency range considered.

The given procedure can be used for a successive specification of the model from Fig. 6 such that its behavior is more accurate within the wider frequency range. On the other hand, the practical frequency range of the CM operation is naturally limited by the bandwidth of the active elements, so the error analysis above this range is not effective.

4.3 CM from Fig. 3b

A similar error analysis as in Sect. 4.2 was also used for the CM from Fig. 3b. The multiplication factor was set by $R_1 \approx 20$ kΩ and $R_2 \approx 1$ kΩ to ca 22; thus, $C_{\mathrm{mul}} \approx 2.2$ nF. The symbolic analysis yields a complex s-domain impedance formula with five zeros and six poles.

It is obvious from Fig. 5b that the frequency characteristics of the emulated impedance are of a similar type as for the CM in Fig. 3a, but with a more obvious parasitic peak in the frequency region below 10 MHz. It follows from the analysis that this peak can be decreased and thus the CM bandwidth increased via increasing the transconductance g_{m0}. It should be done selectively with regard to the circuit tendency to be unstable for high transconductances.

The approximation of the frequency response up to ca 1 MHz, which corresponds to the blue curves in Fig. 5b, can be found as the formula

$$Y = \frac{1}{R_x} + sC_x + sC\frac{R_1 + R_2 + \alpha_0 g_{m0} R_z R_2 + 2\alpha_0 g_{m0} R_z R_1 + sR_z C_z (R_1 + R_2)}{R_1 + R_2 + \alpha_0 g_{m0} R_z R_1 + sR_z C_z (R_1 + R_2)}. \tag{8}$$

Equation (8) can be again arranged to the form (6), where

$$C' = \frac{C}{\frac{R_1}{R_1+R_2} + \frac{1}{\alpha_0 g_{m0} R_z}}, \quad R_{\mathrm{s}} = \frac{C_z}{C\alpha_0 g_{m0}}. \tag{9}$$

This CM can be therefore described by the same model in Fig. 6 as for the circuit in Fig. 3a with the same serial resistance R_{s}, but the capacitance C' is now governed by Eq. (9), not (7). The first Eq. (9) confirms that if the parasitic resistance R_z is high enough, the multiplication factor for this CM does not depend on the transconductance of the CDTA.

4.4 Multiplication Factor Versus CM Bandwidth

The useful frequency range and the capacitance multiplication factor are two conflicting parameters in the C-multiplier design. Most of the CM circuit designs are a compromise between the frequency range and the CM factor. It should be noted here that the permissible operating frequency range is only around one decade in a single op-amp-based CM circuit at a fairly common value of the C-multiplication constant used in IC chip design. Attempts to widen the frequency band of operation in the op-amp-based capacitance multiplier circuit cause a severe reduction in the multiplication factor.

As shown in Sects. 4.2 and 4.3, there is a natural low-frequency limitation of the CM operation caused by parasitic resistance in parallel to the CM terminals (see Fig. 6). This limitation is common to all the existing CMs. Since the corresponding cutoff frequency depends on the RC product, one should make R, in our case the parasitic R_x resistance of the x terminal of the CDTA, as high as possible.

The above error analysis revealed that, in addition to the limited bandwidth of the CDTA, which should be chosen such that it covers well the frequency range of the CM operation, the crucial limiting factors are parasitic impedances of the CDTA terminals. An analysis of the multiplication factor vs the CM bandwidth can be done via the CM model in Fig. 6, which holds for both CMs in Fig. 3.

Let us define the multiplication factor m as

$$m = \frac{C_{\mathrm{mul}}}{C}, \tag{10}$$

where C_{mul} and C are the capacitances after and before the multiplication.

In the ideal case, the multiplication factors for CMs in Fig. 3a, b follow from Eqs. (1) and (2):

$$\mathrm{a}: \quad m = 1 + g_m R, \tag{11}$$

$$\mathrm{b}: \quad m = 1 + \frac{1}{k} = 2 + \frac{R_2}{R_1}. \tag{12}$$

Taking into account that $R_x \gg R_{\mathrm{s}}$ in Fig. 6, it is obvious that the upper limit ω_{U} of the correct frequency behavior of the CM is given by the cutoff frequency of the $C'R_{\mathrm{s}}$ cell. Considering Eqs. (7), (9), (11), and (12), these limits for the CMs in Fig. 3a, b are

$$\text{(a)} \quad \omega_{\mathrm{U}} = \frac{1}{RC_z} = \frac{g_{m0}}{(m-1)C_z}, \tag{13}$$

$$\text{(b)} \quad \omega_{\mathrm{U}} = \frac{\alpha_0 g_{m0} k}{C_z} + \frac{1}{R_z C_z} = \frac{\alpha_0 g_{m0}}{(m-1)C_z} + \frac{1}{R_z C_z}. \tag{14}$$

It is obvious from Eqs. (13) and (14) that the common factor limiting the bandwidth of both CMs is the nonzero parasitic capacitance of the z terminal and that the cutoff frequency is indirectly proportional to the multiplication factor. The bandwidth of the CM in Fig. 3b is higher by the pole frequency of the parasitic $R_z C_z$ cell. Maximizing the upper frequency for both CMs in Fig. 3 with a fixed multiplication factor means to select the transconductance as high as possible and to maintain C_z as low as the CDTA implementation makes it possible. For the CDTA parameters given in Sect. 4.1 and for $m \approx 20$, the upper frequency (13), (14) of both CMs is ca 852 kHz. Note that the $R_{\mathrm{s}}C'$ cell in Fig. 6 introduces a parasitic phase shift of 45° at its cutoff frequency, which causes a deflection of the phase shift of the CM from its ideal value of $-90°$. As a good rule of thumb, the estimated upper limit of the CM operation near the ideal phase shift of a capacitor is one decade below ω_{U}. Then, the phase error will be below 6°.

5 Experimental Results

The CMs from Fig. 3 were constructed via an on-chip CDTA manufactured in CMOS 0.7 μm [6], and their operation was experimentally verified. From among several

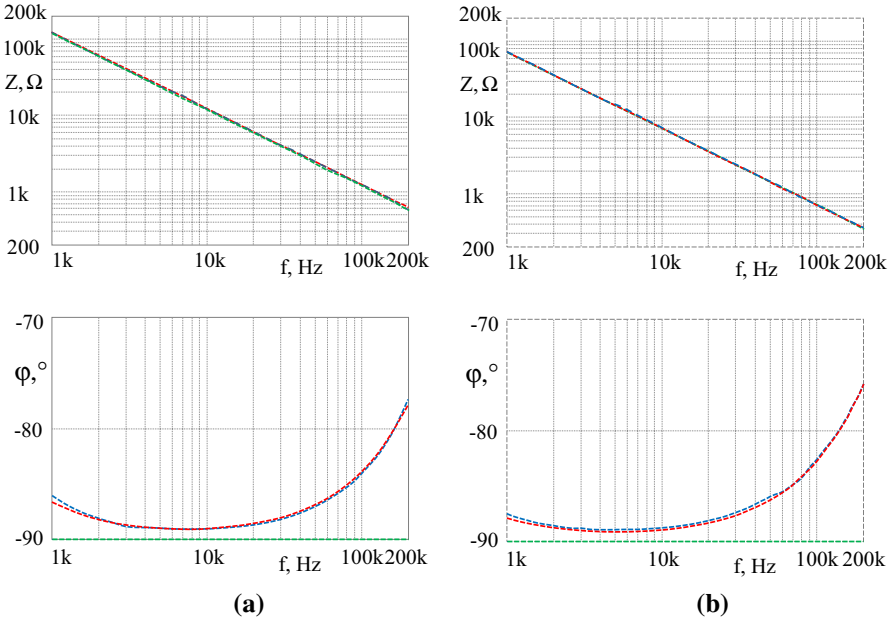

Fig. 7 Modulus and phase of the impedance emulated by the circuit from **a** Fig. 3a, **b** Fig. 3b: red dashed line—simulated characteristics of behavioral symbolic CM model, blue dashed line—measured impedance emulated by the CM, green dashed line—measured impedance of passive capacitor in CM divided by the multiplication factor m. **a** $g_m R+1 \approx 13$, **b** $2+R_2/R_1 \approx 22$ (Color figure online)

CDTA versions appearing on the chip, the type with the parameters given in Sect. 4.1 was selected. Other CM components, i.e., the passive capacitor and auxiliary resistors, were also selected in accordance with the data in Sect. 4. The capacitance C was determined as 100.9 pF on 10 kHz. The impedance of the passive capacitor and also that of both CMs versus frequency were measured via the programmable LCR bridge Rohde&Schwarz HAMEG HM8118 from 1 to 200 kHz. All measurements were exported to the SPICE and compared with the simulations. In addition, also the DC impedances of both CMs were measured and found to be ca 2 MΩ. It conforms to the model from Fig. 6, where the DC impedance is equal to the parasitic resistance of the x terminal of the CDTA.

The measurements for the CMs from Fig. 3a, b are summarized in Fig. 7a, b. Both the modulus and phase of the emulated impedances are in a good match with the behavior of the symbolic models (6), (7), and (9) which evaluate the real effects. All these characteristics also correspond well with the measured modulus of the impedance of the passive capacitor C, divided by the corresponding multiplication factor defined by Eqs. (1) and (2). It follows from the error analysis that the low- and high-frequency deflections of the phase characteristic from the ideal $-90°$ are caused in particular by the parasitic resistance R_x and the parasitic capacitance C_z of the CDTA, respectively.

In order to verify the CM operation, its floating version in Fig. 4b was used for the construction of the second-order low-pass filter in Fig. 8. The corresponding passive

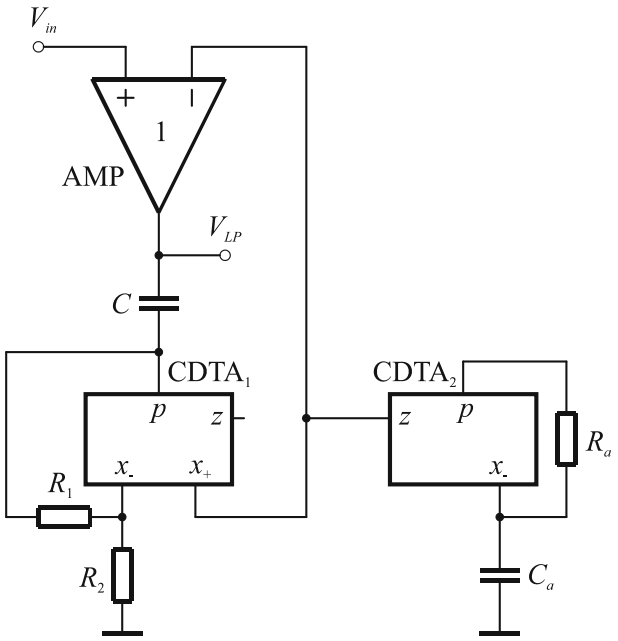

Fig. 8 Experimental second-order low-pass filter

counterpart consists in a serial resonance CLR circuit. The floating capacitor is emulated by the CM between the inputs of AMP, and the LR circuit is made up of the CDTA$_2$ and the R_a C_a cell. The differential input voltage of AMP is copied to the V_{LP} terminal, which therefore serves as the low-impedance low-pass output. A comparison of Figs. 8 and 4b shows that the interconnection of the x terminal of the CDTA and the input terminal V_{in} was removed in the filter in Fig. 8. It simplifies the circuitry without violating its proper operation as active filter. This asymmetry provides a high-input impedance of the V_{in} terminal, concurrently preserving the current excitation of the remaining CDTA$_2$-based LR circuitry. A simple analysis of the circuit containing the CDTA$_2$, R_a, and C_a shows that its impedance Z_z at the z terminal of the CDTA$_2$ is

$$Z_z = \frac{1}{g_{m2}} + sL_z, \tag{15}$$

where

$$L_z = \frac{R_a C_a}{g_{m2}} \tag{16}$$

and g_{m2} is the transconductance of the CDTA$_2$.

Because the CM in Fig. 8 emulates the capacitance C_{mul} (see Eq. (2)) operating between the input terminals of AMP, the corresponding transfer function of the filter in Fig. 8 is

$$K_{\mathrm{LP}} = \frac{\omega_0^2}{s^2 + sB + \omega_0^2}, \tag{17}$$

where the characteristic frequency ω_0, bandwidth B, and quality factor $Q = \omega_0/B$ are

$$\omega_0 = \frac{1}{\sqrt{L_z C_{\mathrm{mul}}}}, \quad B = \frac{1}{g_{m2} L_z}, \quad Q = g_{m2}\sqrt{\frac{L_z}{C_{\mathrm{mul}}}}. \tag{18}$$

Substituting (16) and (2) into (18) yields

$$\omega_0 = \sqrt{\frac{k g_{m2}}{R_a C_a C}}, \quad B = \frac{1}{R_a C_a}, \quad Q = \sqrt{k g_{m2} R_a \frac{C_a}{C}}. \tag{19}$$

The circuit idea in Fig. 8 can be helpful in troubleshooting the well-known problem of designing low-frequency biquads without the use of high-C floating capacitors. Due to the CM in the circuit, a big floating C_{mul} is replaced by a smaller pseudo-grounded C, where $C = k\, C_{\mathrm{mul}}$, $k = R_2/(R_1 + R_2)$. Then, the ω_0 and also Q are decreased by the root of k with regard to the case without the use of CM. The quality factor can then be increased, if necessary, by increasing the $g_{m2}R_a$ product. For a more pronounced decrease in working capacitances, the capacitor C_a can also be implemented as a result of the multiplication of the grounded CM in Fig. 3.

The filter was designed with the following parameters: $C = C_a \approx 100$ pF, $R_a = 328$ kΩ. The multiplication factor was chosen as $m = 100$. It was implemented by $R_1 = 9.9$ kΩ and $R_2 = 100$ Ω. Since the on-chip CDTA provides $g_m \approx 1.22$ mS, the characteristic frequency and quality factor are ca 9.7 kHz and 2, respectively. The difference amplifier AMP was implemented via a 1.5 MHz instrumentation amplifier AD8220 with symmetric power supplies ± 5 V. Frequency responses in Fig. 9 exhibit a good match with the ideal transfer function (17) up to ca 100 kHz (amplitude response) or 20 kHz (phase response). Imperfections above these frequencies are given by the parasitic transfer zero at a frequency of ca 200 kHz, caused by the resonance of parasitic capacitance of the $x+$ and z terminals of the CDTA 1 and 2 (together ca 22 pF) and the inductance L_z (ca 27 mH).

6 Conclusions

Two versions of grounded CDTA-based capacitance multipliers and their possible simple extensions to floating types are proposed in the paper. The advantage of the first version is the utilization of the CDTA with only one current output. The second one requires a double-output CDTA with unwired z terminal. Then, this CDTA works as an ideal current operational amplifier with infinite current gain. It brings some advantages

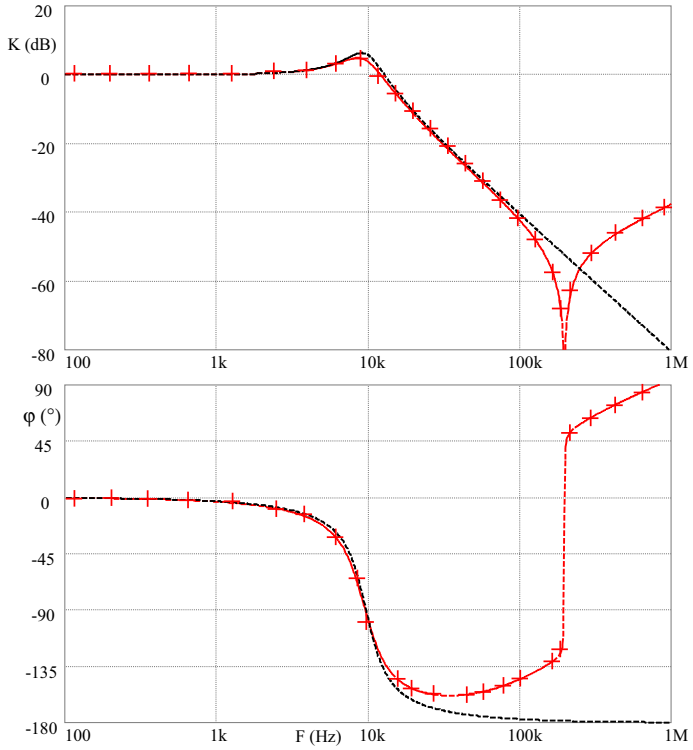

Fig. 9 Frequency characteristics of the filter in Fig. 8: _____ ideal, ---+--- experimental

in comparison with the first circuit, particularly extra low sensitivities to the parasitic resistance R_p of p terminal and also to the transconductance and its thermal variations. The multiplication factor for the first version depends on the $g_m R$ product, whereas for the second CM it is governed by the ratio of two resistors of the current divider.

The intimate error analysis of both CMs can help in revealing the boundary values of the CDTA parameters specified in Sect. 4.1 that warrant the relevant behavior of the circuit within the specified frequency region. The grounded versions, constituting the basis for a possible extension to the floating CMs, were implemented with the help of on-chip integrated CDTAs. The corresponding impedance measurements were in good agreement with the intended behavior of these circuits. Experiments on the second-order active filter also confirmed the proper operation of the floating type of the proposed CM.

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